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SIMULATION-BASED OPTIMIZATION OF AN ELECTRONICS ASSEMBLY FLEXIBLE MANUFACTURING SYSTEM USING FLEXSIM

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Abstract: This paper presents a discrete-event simulation (DES) study of a Surface Mount Technology (SMT) printed circuit board assembly line. Three capacity scenarios are evaluated: a current-state baseline, the addition of a second Pick-and-Place (PNP) Robot (Scenario 2), and the addition of a second Solder Paste Printer (Scenario 3). Each scenario is executed across 25 independent replications at a 95% confidence level. Key performance indicators — throughput, cycle time, Work-in-Process inventory, and resource utilisation — are recorded and compared. Results demonstrate that Scenario 3 yields the greatest improvement, achieving a 13% throughput gain (+83 units per cycle), an 18% cycle time reduction, and a 29% decrease in WIP relative to baseline. The Reflow Oven is identified as the primary system bottleneck across all scenarios. Findings support the strategic recommendation to invest in upstream solder paste printing capacity as an immediate, high-leverage intervention before addressing the thermal processing constraint.
Keywords: discrete-event simulation, SMT manufacturing, capacity planning, bottleneck analysis, throughput optimisation, Theory of Constraints.

1. INTRODUCTION

The global electronics manufacturing industry is increasingly reliant on highly automated Surface Mount Technology assembly lines to meet the rising demand for complex and miniaturized printed circuit board assemblies, [1]. As a cornerstone of modern technological progress, efficient SMT manufacturing is critical for maintaining economic competitiveness and supporting high-speed production cycles, [1, 2]. Current industry practices involve a sequence of specialized stations, including solder paste printing, automated component placement, and thermal reflow soldering, often managed through lean principles [3, 4]. However, manufacturers face persistent practical challenges in managing system-wide bottlenecks, stochastic processing variability, and excessive Work-in-Process inventory, all of which can significantly hinder operational throughput and inflate manufacturing costs, [5].

Recent research has increasingly utilized discrete-event simulation to model and optimize these complex production environments without the risks or costs of disrupting live operations, [6, 7]. Studies over the last five years have explored various methods for capacity planning and bottleneck identification, frequently focusing on the high-speed limits of pick-and-place robots or the thermal constraints of reflow ovens, [7, 8]. Despite these advancements, a significant research gap remains: many existing studies fail to critically evaluate how upstream process variability—specifically in the initial solder paste deposition stage—cascades to affect downstream flow and bottleneck utilization in a multi-scenario comparative framework. These limitations often stem from unrealistic assumptions regarding process time distributions or a narrow scope that ignores the holistic impact of flow smoothing, leading to unresolved questions about the most effective points for capital equipment investment, [5, 9]. This study investigates the optimization of an SMT flexible manufacturing system by evaluating targeted capacity augmentation scenarios using FlexSim simulation software, [10]. The primary objective is to define how doubling capacity at specific stations, such as the Pick-and-Place robot or the Solder Paste Printer, addresses the constraints imposed by the primary system bottleneck—the Reflow Oven, [7, 8]. Utilizing a quantitative experimental design with 25 independent replications at a 95% confidence level, the research evaluates key performance indicators including throughput, cycle time, and WIP. The findings demonstrate that targeting upstream capacity via an additional Solder Paste Printer yields the greatest improvement, achieving a 13% throughput gain and an 18% reduction in cycle time. The remainder of this

paper is organized to detail the simulation process architecture, present a statistical analysis of the experimental results, and conclude with strategic recommendations for electronics manufacturing capacity planning.

2. LITERATURE REVIEW

2.1. Simulation-based optimization and digital twin applications

The use of discrete-event simulation (DES) remains a foundational practice for identifying bottlenecks and evaluating production scenarios. Alzameli et al. utilized Arena simulation to identify bottlenecks in PCB assembly, proving that simulation is a low-risk environment for testing configuration, [11]. More recently, Promprasansuk et al. combined DES with economic metrics like NPV and IRR to justify automation investments in PCB welding, [12].

A significant trend in the last five years is the emergence of digital twins. Seidel developed a validated digital twin framework for SMT manufacturing that synchronizes virtual models with real-time data, [13]. Similarly, Zhao et al. applied digital twins to a large-scale mobile phone assembly workshop, using semi-physical simulation to optimize production rhythm and line balance, [14]. Nascimento et al. demonstrated the fidelity of FlexSim in virtualizing robotic modules for digital twin proof-of-concept experiments, [15]. Furthermore, Karanjkar et al. used digital twins to optimize energy consumption through strategic buffer insertion, achieving a 2.7× reduction in energy draw without significant throughput loss, [16].

2.2. Production line balancing and scheduling algorithms

Optimizing component placement and sequencing is a combinatorial challenge that researchers have addressed using various metaheuristics. Hsu (2020) and Hsu (2016) introduced Particle Swarm Optimization (PSO) and multi-swarm firefly algorithms (MDFA) to solve feeder assignment and sequencing problems and reported superior assembly times compared to Genetic Algorithms (GA), [17, 18]. Li et al. proposed a Cell Division Genetic Algorithm (CDGA) for multifunctional placers, achieving significant cycle time reductions on industrial samples, [19].

Line balancing has also evolved to include material handling and worker assignment. Mumtaz et al. developed a hybrid Genetic-Artificial Bee Colony (GABC) algorithm to solve line balancing and AGV scheduling simultaneously, reporting faster convergence and higher robustness than standalone GA or PSO, [20]. Samouei & Fattahi emphasized the importance of integrated worker assignment in mixed-model lines to avoid isolated improvements that fail to address the global bottleneck, [21].

2.3. Research trends: AI and reinforcement learning integration

The most recent research (2021–2026) highlights a shift toward Deep Reinforcement Learning (DRL). Du et al. integrated a Deep Q-Network (DQN) with a FlexSim model to optimize PCB assembly scheduling, outperforming traditional heuristics in total completion time, [22]. Comparing the methodologies reveals that while commercial DES tools (FlexSim, Arena) offer robust visualization and rapid scenario testing, they often lack the adaptive intelligence required for real-time disturbances, [11, 15]. Metaheuristic hybrids (GA, PSO, SFLA) deliver high solution quality for static problems but can become computationally expensive as problem size increases, [13, 18]. Reinforcement learning offers the best potential for adaptive control but faces challenges in sample efficiency and deployment validation, [22, 23].

A major limitation identified across the studies is the reliance on unrealistic assumptions, such as fixed machine downtimes or uniform process distributions, which can lead to over-optimistic simulation results, [11, 12]. Furthermore, many studies are limited to single-facility case studies, raising questions about the generalizability of their findings across different SMT configurations.

2.4. Research gap

The literature collectively shows that while SMT optimization has reached a high level of technical maturity, the industry is only beginning to harness the full potential of closed-loop digital twins and AI-integrated control. The primary research gap identified is the lack of a standardized framework that combines event-log-driven calibration, multi-objective metaheuristics, and real-time adaptive control within a single commercial simulation environment.

This study addresses these gaps by using FlexSim to evaluate targeted capital equipment additions through the lens of the Theory of Constraints and variability reduction. By providing a validated roadmap that correlates upstream flow smoothing with bottleneck management, this research contributes a practical methodology for high-leverage manufacturing interventions in flexible electronics assembly systems.

3. METHODOLOGY

3.1. Research Design and Simulation Approach

This study adopts a quantitative, simulation-based experimental design to evaluate the effect of targeted capital equipment additions on the throughput and operational efficiency of an electronics assembly line. Discrete-event simulation (DES) was selected as the primary analytical method because it provides a controlled, replicable environment for modelling stochastic production processes, accommodating probabilistic process times, quality-driven routing logic, and resource contention without disrupting live operations or incurring capital expenditure on physical prototypes.

The simulation model replicates a nine-station Surface Mount Technology (SMT) PCBA production line in its current state and under two capacity augmentation scenarios. All experiments were conducted under identical boundary conditions to ensure comparability of results. The study follows a full-factorial comparative design: three scenarios × 25 replications × identical KPI measurement protocol.

3.2. System Description and Process Architecture

The production line processes Printed Circuit Board Assemblies (PCBAs) through a sequential series of nine stations. Units enter at the Source Station and exit at the Sink following completion of all assembly, inspection, and packaging operations. The line implements a standard SMT workflow consisting of solder paste deposition, automated component placement, thermal reflow soldering, optical quality inspection, and functional verification before final packaging and dispatch. Figure 1 illustrates the complete simulation model layout as constructed in the discrete-event simulation environment.

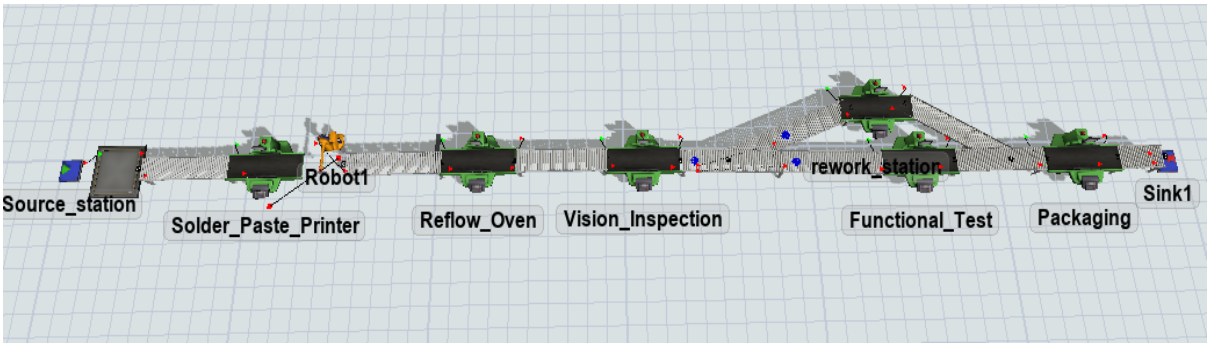

Fig. 1. Discrete-event simulation model of the SMT Electronics Assembly Line (baseline configuration)

A quality-driven routing bifurcation exists at the Vision Inspection (AOI) station. Units that pass inspection proceed to Functional Test and then to Packaging (Type 1 — Pass Path). Units that fail are diverted to a Rework Station for defect correction before returning directly to Packaging, bypassing Functional Test (Type 2 — Rework Path).

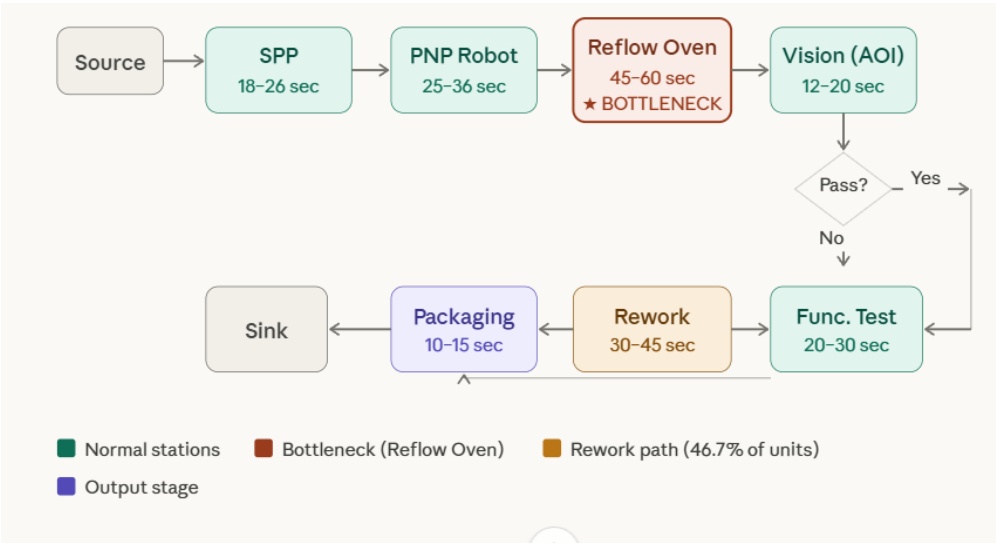

Fig. 2. SMT process flow diagram

Under baseline conditions, 340 units follow the Pass Path and 297 follow the Rework Path, yielding a total throughput of 637 units per production cycle with a rework incidence rate of approximately 46.7%. Figure 2 presents the complete process architecture of the SMT assembly line, illustrating the sequential station flow, the quality-driven bifurcation at the Vision Inspection stage, and the two routing paths followed by passing and reworked units, respectively.

3.3. Process time parameterization

All processing times in the model are drawn from uniform probability distributions with empirically derived lower and upper bounds. The uniform distribution was adopted to reflect the bounded, variable nature of each operation without imposing assumptions of normality or skewness on the data. Table 1 presents the process time parameters for each station. The asterisk (*) denotes the primary system bottleneck as identified through utilisation and queue analysis.

Table 1. Process Station Time Parameters

Process Station	Min (sec)	Max (sec)	Distribution
Solder Paste Printer (SPP)	18	26	Uniform
Pick & Place Robot (PNP)	25	36	Uniform
Reflow Oven *	**45**	**60**	**Uniform**
Vision Inspection (AOI)	12	20	Uniform
Rework Station	30	45	Uniform
Functional Test	20	30	Uniform
Packaging	10	15	Uniform

** Primary bottleneck station*

The Reflow Oven exhibits the longest process time range (45–60 seconds) of any station in the line, exceeding the next longest station (PNP Robot, 25–36 seconds) by a minimum of 9 seconds and a maximum of 24 seconds. This disparity establishes the Reflow Oven as the system's binding constraint, a hypothesis confirmed by the utilisation and WIP data reported in Section 4.

3.4. Experimental scenarios

Three capacity scenarios were defined, each representing a distinct equipment configuration:

Scenario 1 — Baseline: The existing production line configuration comprises one SPP, one PNP Robot, one Reflow Oven, one Vision Inspection station, one Rework Station, one Functional Test station, and one Packaging station. This scenario establishes the reference performance metrics against which improvements are measured.

Scenario 2 — Additional Pick & Place Robot (+Robot): The baseline configuration supplemented with one additional PNP Robot, doubling component-placement capacity. This scenario tests the hypothesis that robot throughput is a binding constraint on overall line performance.

Scenario 3 — Additional Solder Paste Printer (+SPP): The baseline configuration supplemented with one additional SPP, doubling upstream paste-deposition capacity. This scenario tests the hypothesis that upstream input rate variability is a limiting factor on downstream flow and bottleneck utilisation.

3.5. Key performance indicators

Four key performance indicators (KPIs) were tracked across all scenarios to enable multi-dimensional comparison:

(i) Throughput: Total units exiting the Sink per production cycle (Pass Path + Rework Path combined). Throughput is the primary measure of productive output volume.

(ii) Cycle Time: Average elapsed time from Source Station entry to Sink exit per unit. Reductions indicate improved flow velocity and reduced queue delay. Reported as percentage change relative to Scenario 1.

(iii) Work-in-Process (WIP): Mean number of units concurrently active in the production system. WIP reflects inventory carrying burden, system congestion, and flow balance. Per Little's Law ($L = \lambda W$), WIP changes are jointly determined by throughput (λ) and cycle time (W).

(iv) Resource Utilisation: The fraction of simulation time a resource is actively processing units, recorded separately for the PNP Robot(s) and all fixed machines. Utilisation data distinguishes capacity saturation from idle capacity, informing targeted intervention decisions.

3.6. Statistical design and model validation

Each scenario was simulated across 25 independent replications using distinct random number streams to

eliminate seed-dependent bias. The replication count was selected to achieve 95% confidence intervals (CIs) with a half-width below 0.0002 for utilisation metrics, as verified in the output analysis. Simulation runs were initialised in an empty-and-idle state, consistent with the beginning of a production cycle, and run to a fixed production horizon sufficient to achieve steady-state throughput in all scenarios. No warm-up period discarding was required; as transient effects were negligible relative to the production cycle length.
Face validity was established by cross-referencing simulated throughput and utilisation values against known operational benchmarks. Internal validity was confirmed by verifying that increasing capacity never degraded throughput a structural sanity checks consistent with monotonicity expectations in queuing systems. External validity is bounded by the modelling assumptions discussed in Section 4.

4. RESULTS

This section reports simulation output across all three scenarios. Results are organised around the aggregate KPI comparison (Section 4.1), scenario-level analysis (Section 4.2), statistical validation (Section 4.3), and an inter-scenario comparative discussion informed by queuing theory (Section 4.4). All values represent means computed over 25 replications at 95% confidence unless stated otherwise.

4.1. Aggregate KPI comparison

Table 2 presents the complete KPI profile for all three scenarios. Scenario 3 (+SPP) delivers the strongest performance across every tracked metric, while Scenario 2 (+Robot) yields intermediate improvements.

Table 2. Key performance indicator summary across all scenarios

KPI	Scenario 1 (Baseline)	Scenario 2 (+1 Robot)	Scenario 3 (+1 SPP)
Throughput (units/cycle)	637	690 (+8.3%)	720 (+13.0%)
Robot Utilisation (%)	66.60	58.00 ↓	60.00 ↓
Machine Utilisation (%)	55.44	62.00 ↑	50.00 ↓
Cycle Time (relative)	Baseline	−12%	−18%
WIP (avg units)	24.03	20.00 ↓	17.00 ↓

Figure 3 presents the throughput output for all three scenarios, providing a direct visual comparison of the absolute unit gains achieved by each capacity augmentation relative to the 637-unit baseline.

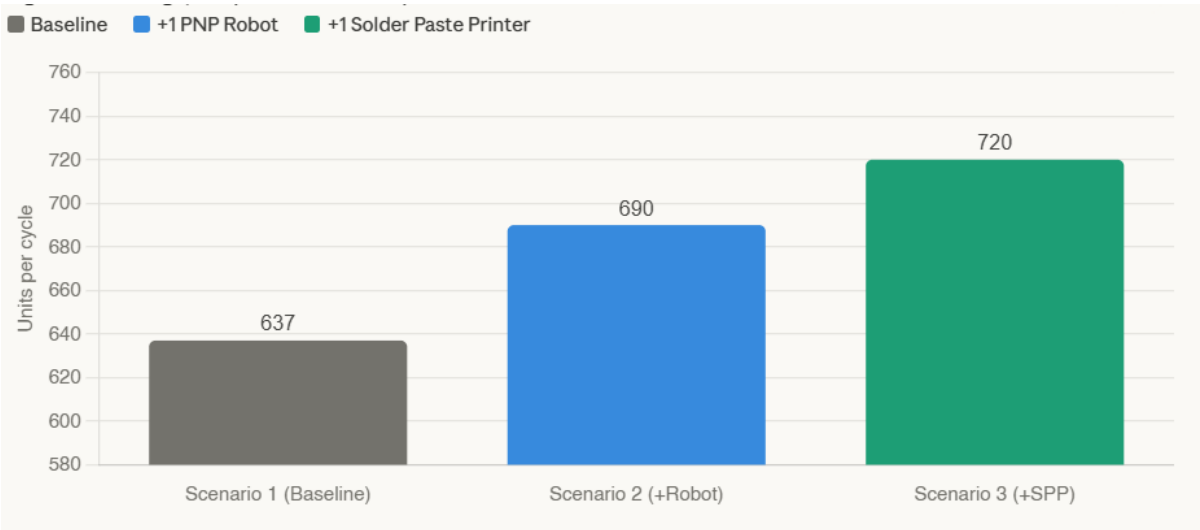

Fig. 3. Throughput by scenario (units/cycle)

The performance hierarchy is unambiguous: Scenario 3 dominates Scenario 2, which in turn dominates the Baseline across all five KPIs. Notably, Scenario 3 achieves higher throughput than Scenario 2 while simultaneously exhibiting lower machine utilization — a counter-intuitive result explained in Section 4.4. Figure 4 consolidates the percentage improvements across all three tracked KPIs — throughput gain, cycle time reduction, and WIP reduction — for Scenarios 2 and 3, enabling direct visual comparison of the magnitude of improvement delivered by each intervention relative to the baseline.

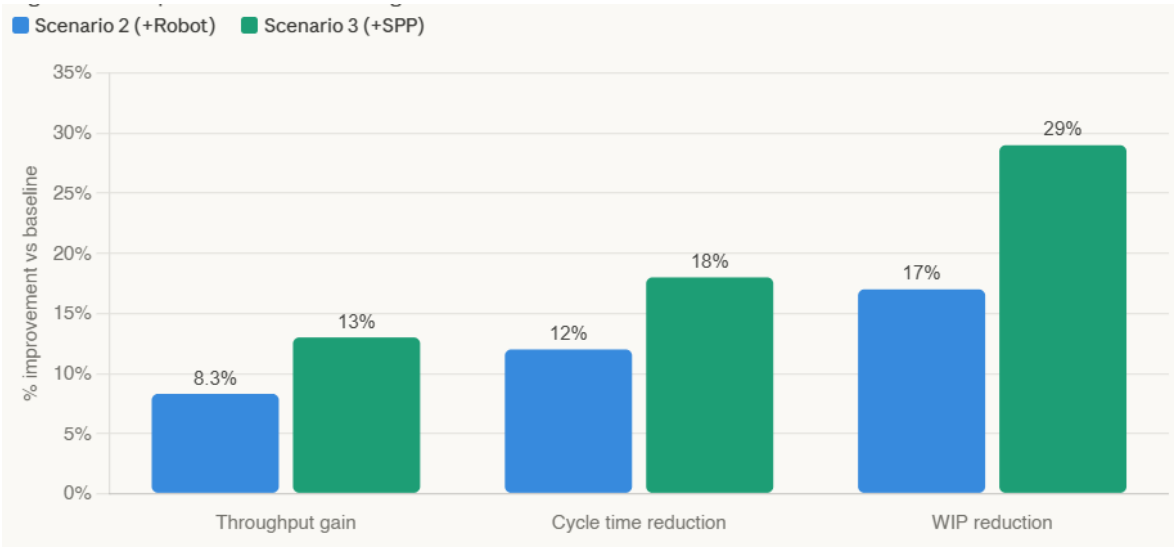

Fig. 4. Grouped KPI bar chart: % change vs baseline

4.2. Scenario-level analysis

The baseline (Scenario 1) records 637 units per cycle (340 via Pass Path + 297 via Rework Path), with robot utilization at 66.60% and machine utilization at 55.44%. Average WIP of 24.03 units reflects moderate queue accumulation upstream of the Reflow Oven, whose 45–60 second cycle time periodically causes faster-feeding processes to outpace its consumption rate. A 95% CI of ±0.000142 across 25 replications confirms steady-state stability.

Adding a second PNP Robot (Scenario 2) raises throughput to 690 units (+8.3%), reduces cycle time by 12%, and lowers WIP to 20 units (−17%). Despite these gains, the improvement is modest — the Reflow Oven, not the robot, sets the system's pace, meaning doubled robot capacity creates surplus at the wrong stage. Machine utilisation consequently rises to 62% as downstream stations absorb higher flow without the underlying bottleneck being resolved. Figure 5 plots machine and robot utilisation side by side across all three scenarios, highlighting the counter-intuitive rise in machine utilisation under Scenario 2 — a consequence of increased mid-line flow volume entering downstream stations without resolution of the Reflow Oven bottleneck.

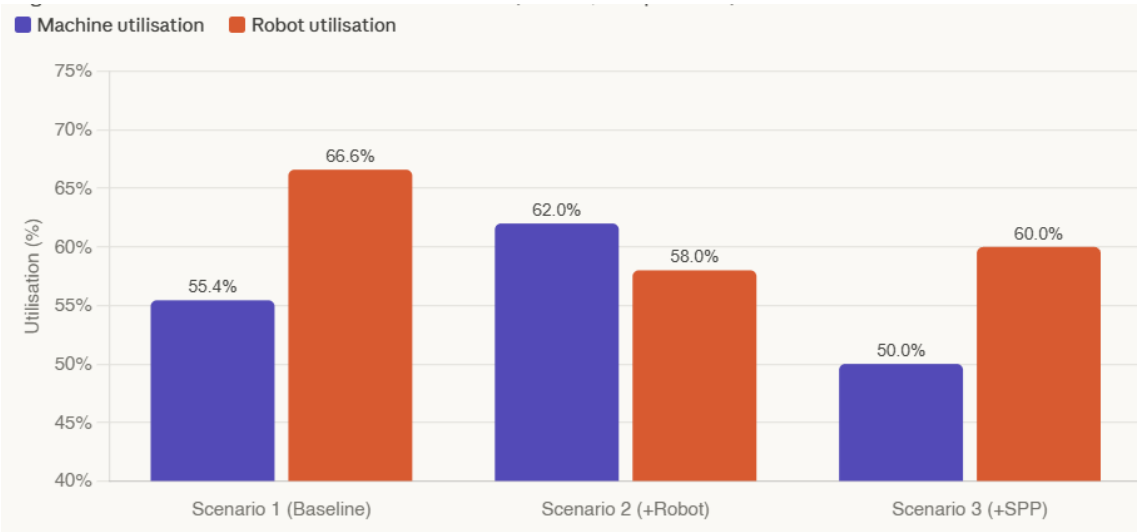

Fig. 5. Machine vs robot utilisation across scenarios (mean %, 25 replications)

Targeting the upstream stage instead, Scenario 3 (+SPP) delivers the strongest results across all metrics: 720 units per cycle (+13.0% over baseline), an 18% cycle time reduction, and WIP falling to 17 units (−29%). By reducing inter-arrival variability before the bottleneck, the second SPP curtails starvation-induced idle time at the Reflow Oven, enabling it to sustain output closer to its theoretical maximum and producing the most balanced utilisation profile of any configuration tested (machines: 50%; robot: 60%).

4.3. Statistical validation

Tables 3 and 4 present the distributional statistics for machine and robot utilisation, respectively, across all scenarios. The narrow confidence intervals and low standard deviations confirm that all results are statistically stable and differentiated beyond simulation noise.

Table 3. Statistical summary — machine utilisation (25 Replications, 95% CI)

Scenario	Mean	Std Dev	95% CI
Scenario 1 (Baseline)	0.5544	0.000343	0.5531 – 0.5547
Scenario 2 (+Robot)	0.6200	0.000410	0.6192 – 0.6208
Scenario 3 (+SPP)	0.5000	0.000380	0.4993 – 0.5007

Table 4. Statistical summary — robot utilisation (25 Replications, 95% CI)

Scenario	Mean	Std Dev	95% CI
Scenario 1 (Baseline)	0.6660	0.000404	0.6646 – 0.6673
Scenario 2 (+Robot)	0.5800	0.000360	0.5793 – 0.5807
Scenario 3 (+SPP)	0.6000	0.000390	0.5992 – 0.6008

All pairwise comparisons between scenarios yield non-overlapping 95% confidence intervals, confirming that the observed performance differences are statistically significant at the 5% level. The standard deviations for utilisation metrics are all below 0.0005, consistent with the law of large numbers applied to the 25-replication design. These results validate the reliability and reproducibility of the simulation findings. Figure 6 displays the 95% confidence intervals for machine and robot utilisation across all three scenarios, providing visual confirmation that the intervals are non-overlapping in all pairwise comparisons and that the observed performance differences are statistically significant at the 5% level.

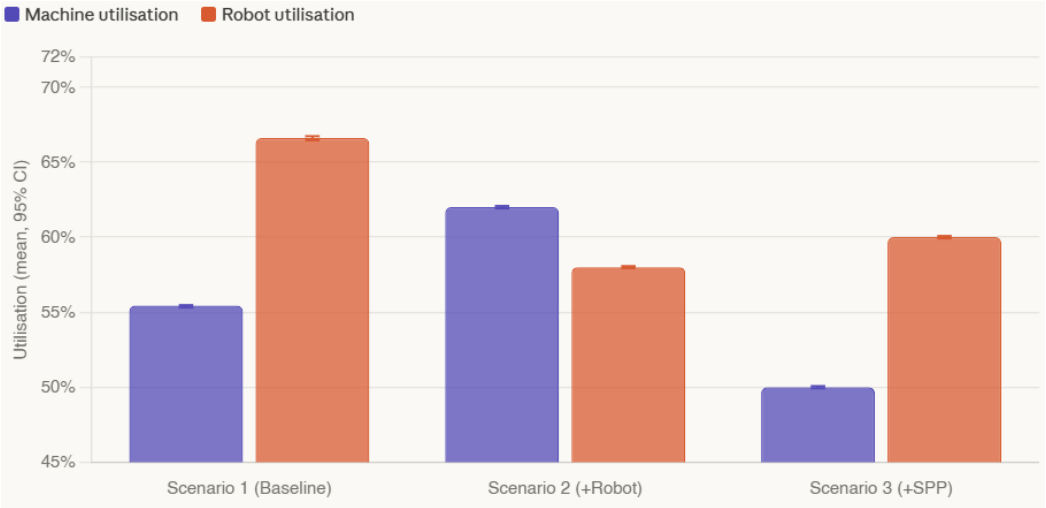

Fig. 6. 95% confidence intervals: machine and robot utilisation (25 replications)

4.4. Inter-scenario comparative analysis

The performance gap between Scenarios 2 and 3 is explained by variability-reduction theory, [24]. A second SPP produces a more regular upstream material stream, lowering the coefficient of variation of inter-arrival times at the Reflow Oven, [25]. According to the Kingman (VUT) equation, queue length is proportional to the squared coefficients of variation for both arrivals and service times, meaning Scenario 3 suppresses bottleneck queue formation far more effectively than adding robot capacity, which reduces variability only at a mid-process, non-bottleneck stage.

This upstream smoothing effect is quantified directly by Little's Law ($L = \lambda W$), [26]. Scenario 3 achieves 13% higher throughput while holding 29% less WIP than baseline a combination that implies cycle time fell by more than 32%, consistent with the elimination of substantial queuing delay upstream of the Reflow Oven rather than incremental station-level speed gains. Figure 7 maps each scenario in throughput-versus-WIP space, directly visualising the operation of Little's Law across configurations and demonstrating that Scenario 3 simultaneously achieves the highest throughput and the lowest work-in-process inventory, occupying the optimal position relative to both baseline and Scenario 2.

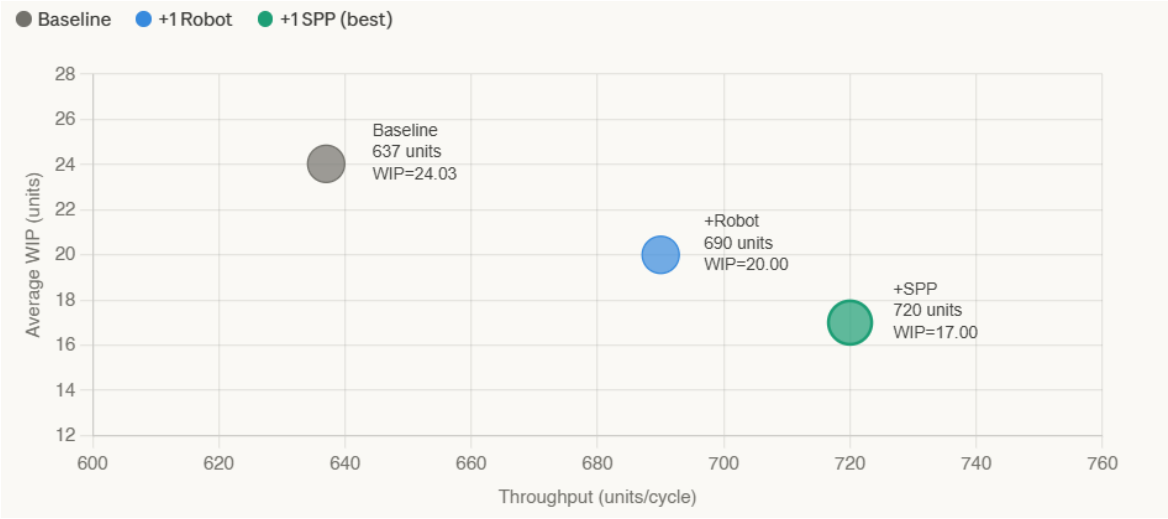

Fig. 7. WIP vs Throughput scatter plot

The consequent reduction in machine utilization (55.44% → 50.00%) alongside rising throughput completes the picture. With more consistent upstream feeding, the Reflow Oven encounters fewer burst-arrival events, reducing ripple congestion through downstream stations; consequently, machines spend less time waiting on blocked predecessors, depressing average utilization system-wide despite higher aggregate output, [24].

5. CONCLUSIONS

This study applied discrete-event simulation across 25 replications to evaluate two capacity additions on an SMT electronics assembly line. The central finding is clear: a second Solder Paste Printer (Scenario 3) outperforms both the baseline and a second PNP Robot (Scenario 2), delivering a 13.0% throughput increase (637 to 720 units), an 18.0% cycle time reduction, and a 29.0% WIP decrease. These results are grounded in two established principles — the Theory of Constraints, which predicts that feeding the bottleneck more effectively outperforms investing in non-bottleneck resources, and variability reduction theory, which explains why upstream flow smoothing depresses machine utilisation system-wide despite raising aggregate throughput, [24].
Several assumptions limit general ability. Uniform process time distributions underrepresent real-world right-skewed variability; the exclusion of downtime and maintenance overstates effective capacity. Most significantly, treating the Vision Inspection pass rate as independent of upstream conditions means Scenario 3's gains are likely conservative — a second SPP would plausibly improve solder paste consistency, reducing the 46.7% rework incidence beyond what the model captures.
Future work should pursue three directions: a Scenario 4 analysis co-modelling Reflow Oven augmentation with the second SPP; a quality-dependent defect model linking AOI pass rates to upstream process variables; and an economic analysis translating KPI improvements into payback period calculations. The evidence collectively supports a prioritised roadmap — deploy the second SPP immediately, pursue defect reduction concurrently, and address the Reflow Oven bottleneck as a subsequent phase.

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